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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/560,717	12/15/2005	Freddy Roozeboom	NL 040226	8503

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EXAMINER	
PHINAZEE, SIDNEY S	
ART UNIT	**PAPER NUMBER**
2815	

NOTIFICATION DATE	DELIVERY MODE
03/20/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/560,717	ROOZEBOOM ET AL.	
	Examiner	Art Unit	
	SIDNEY PHINAZEE	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *2-18-08-*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 December 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This is the initial final office action in reference to application (10/560717), in which claims 1-10 is pending and is taken under consideration at this time.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 3, 5, 7-8, and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chudzik et al (7,030,481) in view of Larson et al (5,495,117).

3. Regarding claim 1 Chudzik discloses an electronic device comprising a semiconductor substrate (200) having a first and a second side and provided with a capacitor and a vertical interconnect (210, 410', 610') through the substrate (200) extending from the first to the second side, on which first side the capacitor is present, characterized in that the capacitor is a vertical trench capacitor (3010) provided with a plurality of trenches in which a layer of dielectric material (3020) is present between a first (3030) and a second (3080) conductive surface (See Fig 3b, 4b, and 6). Chudzik also discloses a layer of insulation (220) between the substrate and feed through. Chudzik discloses both insulation layers can comprise high k dielectric material and accordingly basically anticipates claim 1. Larson also discloses layers of dielectric material being used as insulation between a substrate and the vertical interconnect (Larson reference 20, 26, 36) and other structures of the device. It would have been

obvious to one having ordinary skill in the art at the time of the invention to incorporate the teachings of Larson into Chudzik because it is well known in the art that using dielectric material to isolate conductors and other device structures from one another allows for safe current without arcing.

4. Regarding claim 3 which includes the limitations of claim 1 (addressed above), Chudzik discloses an electronic device, characterized in that the vertical interconnect includes a plurality of parallel trenches each of which is substantially filled with electrically conductive material (230,430).

5. Regarding claim 5 Chudzik discloses an electronic device, characterizes contact pads (240, 270) being present. Chudzik does not explicitly state that the contact pads are for coupling to an external carrier that is present on the second side; or that a first vertical interconnect is used for grounding or that a second interconnect is used for signal transmission.

6. A recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior structure is capable of performing the intended use, then it meets the claim. The applicants intended use of the claimed structure does not structurally distinguish itself over the structure taught by Chudzik. Therefore the recitation of the “a first vertical interconnect is used for grounding” and “second interconnect is used for signal transmission” has not been given patentable weight.

7. Regarding claim 7 Chudzik discloses an electronic device characterized in that an integrated circuit is defined on the second side of the substrate (See Chudzik column 7 lines 57-60).

8. Regarding claim 8, which includes all the limitations of claim 1 (addressed above) Chudzik discloses the substrate to comprise a high ohmic zone (Spec column 7 lines 8-19), which is adjacent to the vertical capacitors and acts as a protection against parasitic currents. (See Fig 3C)

9. Regarding claim 10, which includes all the limitations of claim 1 (addressed above) Chudzik discloses an assembly comprising the electronic device, and a semiconductor device, which semiconductor device (102) is electrically connected to bond pads (270) present on the first side of the substrate.

10. Claims 2,4, and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chudzik (7,030,481) in view of Larson (5,495,117), as applied to claim 1 above, and further in view of Kosaki et al (6,268,619).

11. Regarding claim 2 Chudzik and Larson disclose the limitations of claim 1 but neither reference discloses the limitations of claim 2 of the vertical interconnect, which first part is exposed on the first side of the substrate, is narrower than the second part and has a substantially cylindrical shape. However, Kosaki discloses the vertical interconnect which first part is exposed on the first side of the substrate, is narrower

than the second part and has a substantially cylindrical shape (3) (see figure 14). It would have been obvious to one having ordinary skill in the art at the time the invention to incorporate the teaching of Kosaki with that of Chudzik and Larson because in this sixth embodiment, the anisotropic dry etching as well as the wet isotropic etching form the opening (3). Therefore, in the vicinity of the front surface of the substrate, the opening has a cylindrical shape so that the substrate is not locally thin, thereby suppressing occurrence of cracks. (See Kosaki column 17 lines 10-15)

12. Regarding to claim 4 which include limitations of claim 2 (addressed above) Chudzik discloses an electronic device, characterized in that the first part of the vertical interconnect comprises a plurality of parallel through-holes that extend from the first side of the substrate to the second part of the vertical interconnect each of the plurality of parallel through holes being substantially filled with electrically conductive material (230, 430).

13. Regarding claim 6, which includes limitations of claim 4 (addressed above) Chudzik discloses an electronic device that is characterized in that the first (210) and second (610) interconnect are designed so as to form a coaxial structure.

14. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chudzik (7,030,481) in view of Larson (5,495,117), as applied to claim 1 above, and further in view of Goldberger et al (6,538,300).

15. Regarding claim 9 Chudzik and Larson disclose all of the limitations of claim 8 (as discussed above) Chudzik further teaches the high ohmic zone (Spec column 7 lines 8-19). But neither reference discloses all limitations of claim 9 that characterizes a planar capacitor that is present on the first side of the substrate, which planar capacitor comprises the same layer of dielectric material as the vertical capacitor. However, Goldberger discloses an electronic device, characterized in that a planar capacitor is present on the first side of the substrate, which planar capacitor (10) comprises the same layer of dielectric material (104) as the vertical capacitor. It would have been obvious to one having ordinary skill in the art at the time the invention to incorporate the teaching of Goldberger with that of Chudzik and Larson because capacitors in accordance with Goldberger's invention exhibit numerous advantages. For example, they can be fabricated at a wafer level with a very low effective series resistance (ESR). (See Goldberger column 1 paragraph 8).

Response to Arguments

Applicant's arguments filed February 8, 2008 have been fully considered but they are not persuasive because applicant's arguments on page 6 and 7 stating that " the cited portions of the Chudzik and Larson references do not correspond to the claimed invention which includes, for example, aspects directed to a layer of dielectric material, which is used as the dielectric of a vertical trench capacitor and also as insulation between a substrate and a vertical interconnect that extends through the substrate, are not convincing. In actuality, Larsen teaches that these insulating layers (20, 26, and 36)

are deposited over a transistor 10, which is fabricated on a substrate. See, e.g., Col. 3:46-57. The cited portions of Larson do not mention any vertical interconnect that extends through this substrate or that Larson's insulating layers (20, 26, and 36) are used as insulation between this substrate and some apparently nonexistent vertical interconnect. The cited portions of Larson also do not mention that these insulating layers (20, 26, and 36) are used as the dielectric in a vertical trench capacitor. Accordingly, the cited portions of Larson do not teach that insulating layers (20, 26, and 36) form the dielectric of a vertical trench capacitor or that these insulating layers provide insulation between a substrate and a vertical interconnect that extends through the substrate. Applicant notes that the Chudzik reference already discloses that there is an insulating material 220 between the substrate 200 and the conductive material 230 in the via 210. See, e.g., Figure 3b and Col. 4:13-15. However, applicant argues Chudzik's insulating material 220, which separates the conductive material 230 from the substrate 200, is not the same layer that is used as the dielectric film 320 of trench capacitor structures 3010. Accordingly, the cited portions of Chudzik do not teach that the same layer of dielectric matter is used as both the dielectric of a vertical trench capacitor and to provide insulation between a substrate and a vertical interconnect that extends through the substrate."

In actuality Chudzik does teach the dielectric 3020 being the same material (high k dielectric) as the feed through dielectric layer 220 and 420' (high k dielectric) (Chudzik column 5 lines 11-15 and column 6 lines 19-22) and accordingly is basically anticipating art. Nonetheless, Larson additionally discloses several insulation layers of the same

material in a single semiconductor device and suggests using the same insulation material for several insulation layers in a single device as Chudzik for ease of manufacture and reliability. Therefore the invention is not patentable over Chudzik and Larson.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SIDNEY PHINAZEE whose telephone number is (571)270-5020. The examiner can normally be reached on Mon-Fri 7:30-5:00 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Parker can be reached on 571-272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SSP

/Jerome Jackson Jr./
Primary Examiner, Art Unit 2815